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Effect of Doping of MLGNR on Propagation Delay of a Driver-Interconnect-Load system

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ABSTRACT
Nowadays multi layer GNR (MLGNR) is used in nano scale VLSI interconnection. In this research paper study has been done on two variants of MLGNR, one neutral MLGNR (means with no doping) and second intercalated doped MLGNR, in terms of propagation delay. The test circuit which has been used to check the propagation delay is a Driver-interconnect-load system which is using CMOS, short gate (SG) FinFET, independent gate (IG) FinFET, and low power (LP) FinFET as driver and load circuits at 16 nm.
Keywords - CMOS , Driver-interconnect-load system , FinFET , Multi layer GNR.

I.   INTRODUCTION

In past some work has been done by the researchers on neutral and intercalated doped MLGNR [1][2]. In neutral MLGNR layers are separated with a distance of 0.34 nm, if a MLGNR is doped with AsF_5 its conductivity increases reason behind that is due to intercalation doping density of carriers increases due to which mean free path increases [3]. Also the inter layer spacing increases due to doping [3][4].
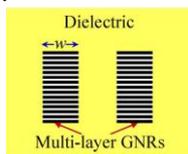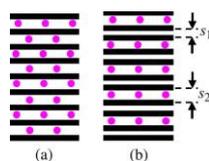

Fig. 1 Schematic view of neutral multilayer GNRs [2]

Fig. 2 Schematic view of two types of intercalated GNR s1 and s2 are the layer spacing between two adjacent graphene layers. In stage-2 AsF_5 intercalated graphite, s1 = 0.335 nm and s2 = 0.815 nm [5].

Conductance of MLGNR can also be increased by making the edges of GNR specular. But in this work only intercalation doping has been considered which makes $E_F = 0.6eV$ and mean free path 1.03 µm. For a neutral MLGNR mean free path is 0.4 µm [6]. For a neutral MLGNR $E_F = 0.1eV$ has been considered in this work.

In this paper propagation delay has been studied for both the variants of MLGNR described in previous paragraph. The simulation test circuit is a driver-interconnect-load system which uses four different drivers and loads. The work has been performance at 16 nm.

The paper has four sections, first section gives brief about the aim of work, second section gives the RLC model of MLGNR, third section presents result and forth section is conclusion of work.
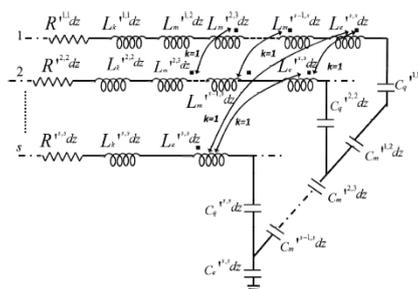
II.   RLC MODEL OF MLGNR

Fig. 3: RLC circuit for MLGNR [7]

The capacitances and inductances of equivalent model which includes electrostatic capacitance, quantum capacitance and mutual capacitance, kinetic inductance, electrostatic inductance and mutual inductance are given by the expressions [2][8][9].

$$C_Q = N_{ch}N_{layer} \, 4q^2/hv_f = N_{ch}N_{layer} * 193.18 \, aF/\mu m \quad (1)$$
$$C_E = \varepsilon_0 * w/d \; aF/\mu m \quad (2)$$
$$C_{m,layer}^{(j-1,j)} = \varepsilon_0 * (w/\partial) \; aF/\mu m \quad (3)$$
$$L_K = (h/4q^2 v_f)/ N_{ch}N_{layer} = 8.0884/ N_{ch}N_{layer} \; nH/\mu m \quad (4)$$

$$L_E = \mu_0 * (d/w) \; nH/\mu m \quad (5)$$
$$l_{m,layer}^{(j-1,j)} = \mu_0 * (\partial /w) \; nH/\mu m \quad (6)$$

The quantum resistance and scattering resistance is given by [10],

$$R_Q = (h/2q^2)/N_{ch}N_{layer} = 12.94 \; K\Omega/ N_{ch}N_{layer} \quad (7)$$
$$R_S = R_Q / \lambda \quad (8)$$

Where λ = mean free path.

In MLGNR the values of quantum resistance, quantum capacitance and kinetic inductance are depend on number of conducting channels in GNR layers which further depend on width and E_F of GNR. The value of conducting channels has been calculated by the expression given by Nasiri in [8].

III.   SET UP AND RESULT

The set up which has been used for simulation is a DIL system with CMOS,SG FinFET, IG FinFET, and LP FinFET driver-load stage.
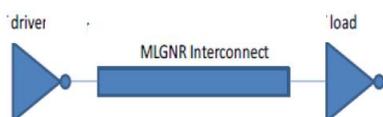
Fig. 4: Simulation Setup

The delay effect has been measured and compared for both variants of MLGNR i.e, for neutral MLGNR and for doped MLGNR. Fig. 5 to Fig. 7 gives the clear comparison between doped and neutral GNR when used with a driver-load stage for super threshold region, near threshold region and sub threshold region. Also Fig. 8 shows the delay variation of GNR for both doped and neutral MLGNR with respect to width for all cases of DIL systems.
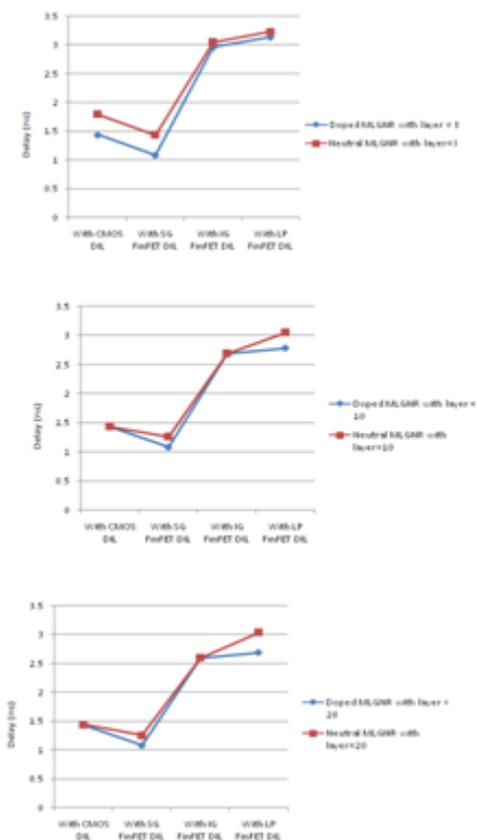
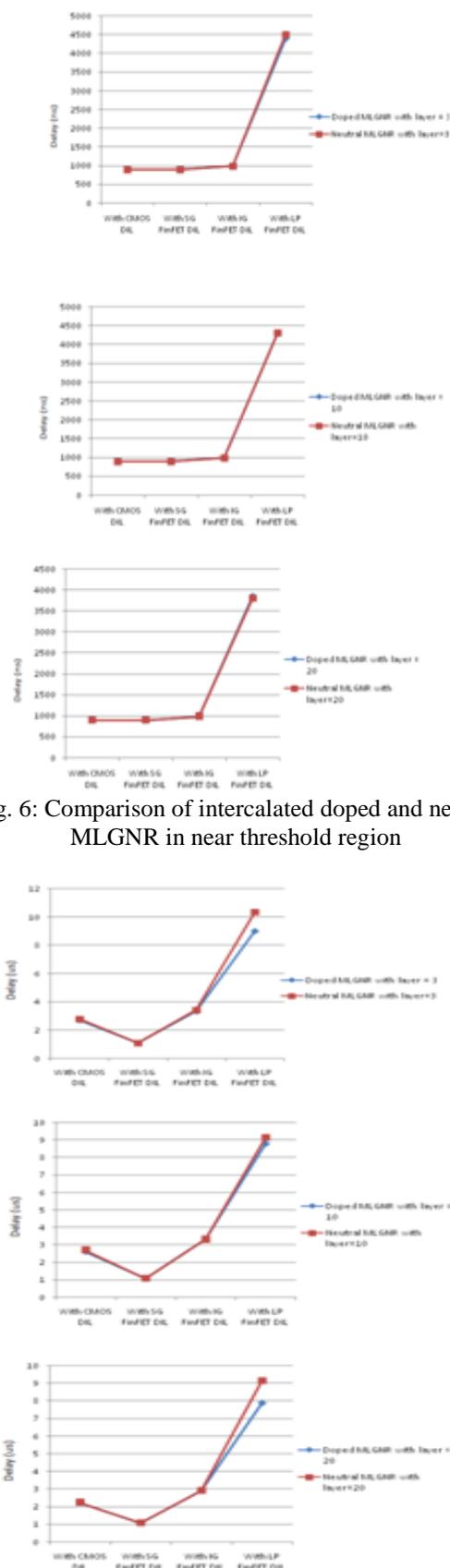Fig. 5: Comparison of intercalated doped and neutral MLGNR in super threshold region

Fig. 6: Comparison of intercalated doped and neutral MLGNR in near threshold region

Fig. 7: Comparison of intercalated doped and neutral MLGNR in sub threshold region
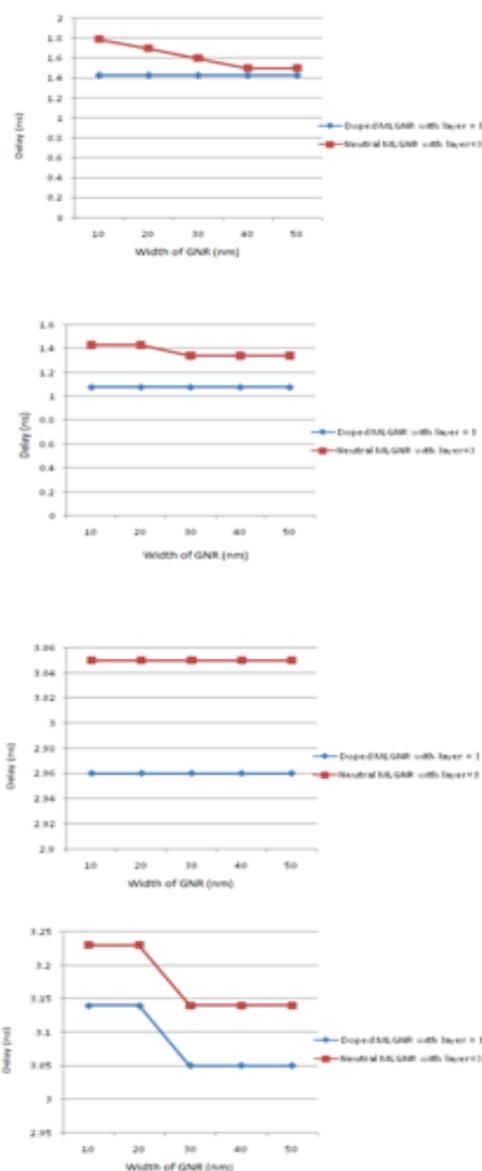
Fig. 8: variation of delay of intercalated doped and neutral MLGNR with respect to width for (a) CMOS driver, (b) SG FinFET driver, (c) IG FinFET driver and (d) LP FinFET driver.

IV.   CONCLUSION

A comparison has been presented between DIL system using doped MLGNR and DIL system with neutral MLGNR and it has been noticed that for DIL system using doped MLGNR propagation delay is less as compared to the DIL system using neutral MLGNR interconnect. And also it has been observed that in near threshold region the comparison effect is not significant.

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